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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,040	02/20/2004	Eric Neyret	4717-10100	1950

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EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 09/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,040	NEYRET ET AL.	
	Examiner	Art Unit	
	Lex Malsawma	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 Feb 2004 through 08 Jun 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 6-14* is/are rejected.

7)☒ Claim(s) *3-5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20040220*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 2 is objected to because of the following informalities:

In line 2, the examiner suggests changing "heated" to "heating".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 10 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Imaoka et al. (5,426,073; hereinafter, "**Imaoka**").

Regarding claims 1 and 13:

Imaoka discloses a preventive treatment method for a multilayer semiconductor wafer that includes a supporting substrate 1 (Fig. 7b), at least one intermediate layer 2 (Fig. 7b) and a surface layer 4 (Fig. 7c) in which an intermediate layer 2 has an exposed lateral edge and the wafer is to be subjected to a subsequent treatment, which method comprises encapsulating the exposed lateral edge of the intermediate layer with a portion of the surface layer 4 to prevent attack on the peripheral edge during the subsequent treatment. Note that the wafer 1 will inherently be subjected to at least a subsequent treatment, e.g., the wafer 1 would be diced/cut to

form individual chips/dies; accordingly, the surface layer 4 (i.e., the passivation layer) will prevent attack on the peripheral edge. *Specifically regarding claim 13:* All recited structural limitations within this claim are included in the method of claim 1. Therefore, Imaoka anticipates claims 1 and 13.

Regarding claim 10:

Imaoka discloses the edge of the intermediate layer 2 is encapsulated/protected by the surface/passivation layer; accordingly, a subsequent treatment would not detrimentally affect the edge of the intermediate layer. Therefore, Imaoka anticipates this claim.

4. Claims 1, 2, 6 and 10-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwamatsu et al. (6,150,696; hereinafter, "**Iwamatsu**").

Regarding claims 1, 6, 13 and 14:

Iwamatsu discloses a preventive treatment method for a multilayer semiconductor wafer (having an SOI structure) that includes a supporting substrate 1 (Fig. 1), at least one intermediate layer 3 (Fig. 9) and a surface layer 23 (Fig. 10) in which an intermediate layer 3 has an exposed lateral edge and the wafer is to be subjected to a subsequent treatment (i.e., etching/chemical attack, note Col. 11, lines 15-20), which method comprises encapsulating the exposed lateral edge of the intermediate layer with a portion of the surface layer 23 to prevent attack on the peripheral edge during the subsequent treatment. *Specifically regarding claims 13 and 14:* All recited structural limitations within these claims are included in the method of claims 1 and 6. Therefore, claims 1, 6, 13 and 14 are anticipated.

Regarding claims 2, 10 and 11:

Iwamatsu discloses the encapsulating comprises annealing the wafer by heating to a temperature and for a time sufficient to cause the surface layer 23 to cover the exposed lateral edge of the intermediate layer 3 (Fig. 10 and Col. 11, lines 2-13). Iwamatsu further discloses subjecting the wafer to the subsequent treatment without detrimentally affecting the edge of the intermediate layer, wherein the subsequent treatment is a chemical attack/etching (note Col. 11, lines 15-20). Therefore, these claims are anticipated.

Regarding claim 12:

Iwamatsu discloses oxidizing the surface of the wafer to create oxide layer(s) "21" and/or "23" (Figs. 8 and 10) on the surface of the wafer by annealing at a temperature of about 1100 °C (Col. 10, lines 46-48); and deoxidation of the oxide is carried out by a chemical attack using a wet etching solution (Col. 11, line 15-20). Therefore, Iwamatsu discloses subjecting the wafer to a "stabox" process (note page 2, lines 14-21, of the current specification for steps used in a "stabox" process).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Iwamatsu** (6,150,696) in view of Applicant Admitted Prior Art, hereinafter, "**AAPA**" (specification pages 1-2).

Regarding claims 7-9:

Iwamatsu anticipates the method of claim 1 but **lacks** specifically disclosing process steps utilized for acquiring the SOI substrate 10 (note Figs. 1-2); accordingly Iwamatsu lacks the limitations recited in claims 7-9. AAPA **teaches** conventional processes for acquiring an SOI substrate include the incorporation of the well-known SMART-CUT® process, where the conventional processes comprise transferring at least a surface layer from a donor wafer to at least one intermediate layer by a layer transfer technique (specification page 1, lines 5-22), wherein the surface layer is transferred by forming a zone of weakness in the donor substrate at a depth sufficient to define the surface layer (specification page 1, lines 6-9 and 21-22), bonding the surface layer of the donor wafer to the intermediate layer of the supporting substrate and then detaching the surface layer from the donor wafer (specification page 1, lines 6-8). AAPA discloses the well-known SMART-CUT® process is used to formed the weakened zone, and it is also very well known that the SMART-CUT® process includes implanting ions to form the zone

of weakness. Since Iwamatsu does not specify a process for acquiring the SOI substrate, it would have been obvious to one of ordinary skill in the art to utilize any well-known process for acquiring the SOI substrate, such as the well-known SMART-CUT® process. Therefore, it would have been obvious to one of ordinary skill in the art to modify Iwamatsu by specifically utilizing a conventional "SOI process" incorporating the well-known SMART-CUT® process to acquire the SOI substrate, especially since the essential inventive aspects in Iwamatsu and the current invention do not depend on process steps for acquiring an SOI substrate, i.e., the inventive aspects essentially pertain to process steps performed after an SOI substrate has been acquired.

Allowable Subject Matter

8. Claims 3-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

Claims 3-5 are allowable primarily because the references of record, singly or in combination, cannot anticipate or fairly suggest a rapid thermal annealing (RTA) process performed at the temperature and time specified in claim 3, wherein the RTA process is sufficient to encapsulate the exposed lateral edge of the intermediate layer and is also sufficient to "provide an encapsulant" that will prevent attack on the peripheral edge during subsequent treatment.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The references listed on the attached Form PTO-892 (not cited above) are cited to show processes for "encapsulating" an edge/peripheral portion of a substrate to prevent attack on the peripheral portion during subsequent treatment(s).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903. The examiner can normally be reached on Mon-Fri (8 hours between 5:30AM and 8:00 PM EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lex Malsawma

September 18, 2004

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
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